Office Action Summary	Application No.	Applicant(s)	
	10/783,181	CORR, WILLIAM E.	
	Examiner	Art Unit	
	Hal D Wachsman	2857	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6* is/are rejected.

7)☒ Claim(s) *7-10* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *19 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2-19-04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. The Cross Reference To Related Applications section on page 1 of the specification does not provide the current status of U.S. application serial no. 10/016,183. Appropriate correction is required.

2. Page 11 of the specification, paragraph 0056, refers to figures 1-7 however there is not a figure 7 but rather there are figures 7A, 7B and 7C. Appropriate correction is required.

3. The Examiner respectfully notes a grammatical error on page 8, paragraph 0042, of the specification: "..of can also be found..."

4. Claims 2-10 are objected to under 37 C.F.R. 1.75(a) for failing to particularly point out and distinctly claim the subject matter which the applicant regards as the invention. Claim 2, line 4, cites "a third test circuit operable to produce a third signal" however there was not a second test circuit and a second signal cited before this in the claim. This same type of problem also occurs in claim 3, line 5, claim 4, lines 2 and 5, claim 5, lines 2 and 5, claim 6, lines 2 and 5. Claim 4, line 3, cites "said plurality of components" which lacks antecedent basis. This same type of problem also occurs in claim 5, line 3, claim 6, line 3. Claim 8, lines 1-2, refer to "a second ring oscillator" however there was not a first ring oscillator cited before this second ring oscillator. This same type of problem also occurs in claims 9 and 10. Claim 8, lines 2-3, cite "said integrated circuit" which lacks clear antecedent basis in claims 4 and 5. Claims 9 and 10, cite "said integrated circuit" which lacks antecedent basis in claim 6. The examiner asks the applicant to better claim the limitations cited above. While the examiner

understands the intentions of the applicant he feels confusion could be drawn from the limitations cited above. Appropriate correction is required.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

6. Claims 1, 2 and 4, are rejected under 35 U.S.C. 102(e) as being anticipated by Stinson et al. (6,553,545).

As per claim 1, Stinson et al. (Abstract, col. 2 lines 40-50, 55-60, col. 3 lines 15-21) disclose a test circuit operable to produce a signal for determining an operating reference signal. Stinson et al. (Abstract, col. 4 lines 8-15, col. 8 lines 15-17) disclose a test circuit operable to produce a signal for determining a cross-talk effect on a plurality of components.

As per claim 2, Stinson et al. (Abstract, col. 2 lines 40-50, 55-60, col. 3 lines 15-21) disclose a test circuit operable to produce a signal for determining an operating reference signal. Stinson et al. (Abstract, col. 2 lines 24-33, col. 3 lines 34-36, col. 4 lines 13-15) disclose a test circuit operable to produce a signal for determining an effect of system noise on the operational speed of the plurality of components.

As per claim 4, Stinson et al. (Abstract, col. 4 lines 8-15, col. 8 lines 15-17) disclose a test circuit operable to produce a signal for determining a cross-talk effect on a plurality of components. Stinson et al. (Abstract, col. 2 lines 24-33, col. 3 lines 34-36, col. 4 lines 13-15) disclose a test circuit operable to produce a signal for determining an effect of system noise on the operational speed of the plurality of components.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 3, 5 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Stinson et al. (6,553,545) in view of Durham et al. (6,532,574).

As per claim 3, Stinson et al. (Abstract, col. 2 lines 40-50, 55-60, col. 3 lines 15-21) disclose a test circuit operable to produce a signal for determining an operating reference signal. It appears though that Stinson et al. does not clearly disclose another test circuit operable to produce a signal for determining an effect of power supply noise on a signal propagation delay within a plurality of components. However, Durham et al. (col.1 lines 25-37, col. 8 lines 8-23) teach this excepted feature. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to apply the techniques of Durham et al. to the invention of Stinson et al. as specified above because as taught by Durham et al. (col. 1 lines 26-29) some common forms of noise are **power supply** droop and localized **power variations**, signal line coupling, and Miller effect capacitances across circuit inputs/outputs.

As per claim 5, Stinson et al. (Abstract, col. 4 lines 8-15, col. 8 lines 15-17) disclose a test circuit operable to produce a signal for determining a cross-talk effect on a plurality of components. It appears though that Stinson et al. does not clearly disclose another test circuit operable to produce a signal for determining an effect of power supply noise on a signal propagation delay within a plurality of components. However, Durham et al. (col.1 lines 25-37, col. 8 lines 8-23) teach this excepted feature. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to apply the techniques of Durham et al. to the invention of Stinson et al. as specified above because as taught by Durham et al. (col. 1 lines 26-29) some common

forms of noise are **power supply** droop and localized **power variations**, signal line coupling, and Miller effect capacitances across circuit inputs/outputs.

As per claim 6, Stinson et al. (Abstract, col. 2 lines 24-33, col. 3 lines 34-36, col. 4 lines 13-15) disclose a test circuit operable to produce a signal for determining an effect of system noise on the operational speed of the plurality of components. It appears though that Stinson et al. does not clearly disclose another test circuit operable to produce a signal for determining an effect of power supply noise on a signal propagation delay within a plurality of components. However, Durham et al. (col.1 lines 25-37, col. 8 lines 8-23) teach this excepted feature. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to apply the techniques of Durham et al. to the invention of Stinson et al. as specified above because as taught by Durham et al. (col. 1 lines 26-29) some common forms of noise are **power supply** droop and localized **power variations**, signal line coupling, and Miller effect capacitances across circuit inputs/outputs.

9. Claims 7-10 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims and subject to the appropriate correction of the 37 C.F.R. 1.75(a) objections noted in paragraph 4 above.

10. The following references are cited as being art of general interest: "On-chip interconnect evaluation on delay time increase by crosstalk" (Yamashita et al.) which disclose the effect of cross-talk on the delay time, Savithri et al. (6,732,339) which disclose full chip cross-talk noise verification, Richer (6,480,986) which discloses IC

substrate noise modeling including extracted capacitance and Hsu et al. (6,349,067) which disclose preventing noise cross contamination between embedded DRAM and system chip.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hal D Wachsman whose telephone number is 571-272-2225. The examiner can normally be reached on Monday to Friday 7:00 A.M. to 4:30 P.M..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Marc Hoff can be reached on 571-272-2216. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Hal D Wachsman
Primary Examiner
Art Unit 2857

HW
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